Short-Circuit Capability Demonstrated for GaN Power Switches

Davide Bisi*, John Gritters*, Tsutomu Hosoda†, Masamichi Kamiyama†, Bill Cruse*, YuLu Huang*, Jim McKay*, Geetak Gupta*, Rakesh Lal*, Carl Neufeld*, Philip Zuk*, YiFeng Wu*, Primit Parikh*, Umesh Mishra*

* Transphorm, Inc., 75 Castilian Dr., Goleta, CA 93117, USA. Corresponding Author: dbisi@transphormusa.com

† Transphorm Japan Inc., 2-5-15 Shin-Yokohama, Kouhoku-ku, Yokohama, Japan

***Abstract*—Short-circuit capability is essential for the adoption of GaN power devices in motor drives for industrial and automotive applications. In this work, we report an innovative solution for GaN power switches to achieve short-circuit withstanding time (SCWT) equal to or greater than 3 micro-seconds with limited increase in on-resistance. We discuss the technology, referred to as Short-Circuit Current Limiter (SCCL) and show the experimental results including static and dynamic R_{on}, 400-V short-circuit, inductive switching, off-state leakage and 1000-hour high-temperature reverse-bias stress. Thanks to extended SCWT, the SCCL technology allows the industry to adopt conventional short-circuit protection schemes, with sufficient immunity to noise and switching transients.**

Keywords—GaN, HEMT, Power Device, Short-Circuit, SCWT, SCCL, Motor Drive, Inverter, Protection Circuit

I. Introduction

High-efficiency GaN power devices are penetrating several power electronics markets, including adapters, power supply units, photovoltaic inverters, battery chargers, and motor drives. Short-circuit capability is an important requirement, especially in motor drives, where power devices may be required to withstand short-circuit events caused by overload, shoot-through, current surge and/or external fault conditions (Fig. 1) [1].

When a short-circuit event occurs, the system must detect the fault and safely turn-off all the power devices to prevent catastrophic failure and ensure safe operations. The fault detection can be added to the gate-driver with protection circuitry such as desaturation detection (DESAT) or over-current sensing (OC) [2]. The response time of the protection circuitry must be carefully tuned: if the response time is too fast, the protection circuitry may be erroneously activated by glitches, noise, and switching transients. If the response time is too slow, the power device may fail before the protection system is activated, posing a dangerous hazard for systems and users. Typically, an adequate response period is in the order of approximately 2 µs [3], enough to filter out glitches and switching transients. During this period, the power device must withstand the short-circuit condition without failing. Hence the need to define a key device requirement: the Short-Circuit Withstanding Time (SCWT), i.e., the minimum time during which a device is capable to withstand a short-circuit event, with both high voltage and high current applied between source and drain terminals. Usually, the SCWT is measured and reported either at the customer operative voltage or at approximately 2/3 of the device maximum rated voltage. For example, for 650-V and 1200-V rated devices, the SCWT is usually tested and reported at 400 V and 800 V, respectively.

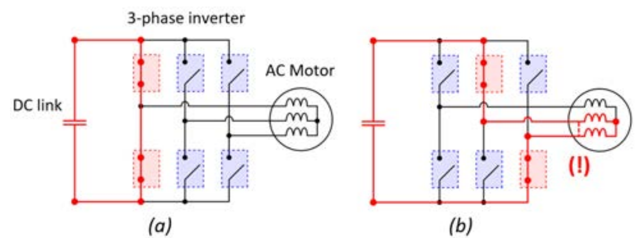

Fig. 1. Power devices employed in a 3-phase motor drive scheme, showing two short-circuit scenarios: *(a)* shoot-throhgh between high-side and low-side and *(b)* short-circuit across the inductive load.

One of the primary factors limiting the SCWT is the thermally induced catastrophic failure [4] [5]. During short-circuit conditions, the device is subjected to both high voltage and high current; a condition that leads to enormous instantaneous power dissipation and rapid increase in temperature, until one or more failure mechanisms are triggered and the catastrophic failure happens (Fig. 2a). To improve SCWT, it is therefore important to limit the power dissipated during a short-circuit event, so that the protection circuitry can intervene before the critical temperature to failure is reached (Fig. 2b). The biggest challenge is doing so while maintaining high device performance (low on-state resistance, low capacitance and fast switching) and long-term reliability.

II. SCWT of WBG Devcices

In conventional silicon-based power-devices, such as Si IGBTs, the SCWT can be greater than 10 µs [6]. On the other hand, ensuring a high SCWT in wide-band gap (WBG) devices such as SiC MOSFETs or GaN HEMTs is more challenging. Due to their own nature and virtue, WBG devices can deliver much higher power density in smaller areas than conventional silicon devices. Consequently, when subjected to short-circuit

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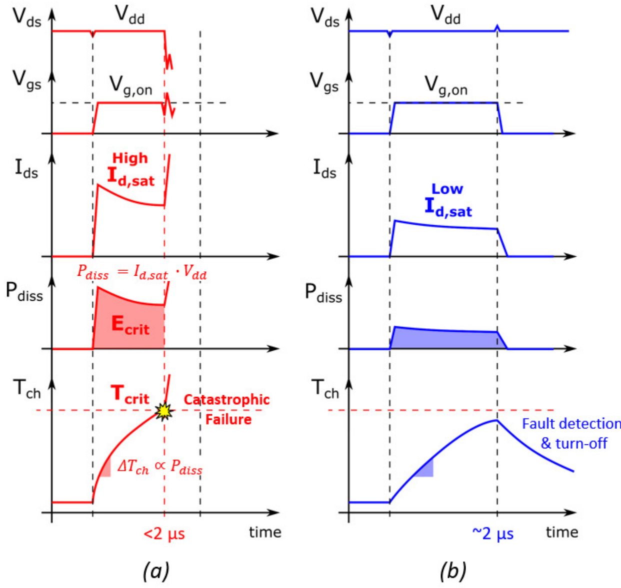

Fig. 2. Schematic waveforms during short-circuit condition for *(a)* a device with high current and power density leading to steep temperature rise and catastrophic failure before the protection circuitry could intervene and *(b)* a device with lower current and lower power density, allowing the protection circuitry to detect the fault and safely turn-off the device before the critical temperature to failure is reached.

conditions, they may experience a steeper rise in temperature resulting in shorter SCWT than silicon-based counterparts.

A. *Overview of SiC Devices*

SiC devices show a strong trade-off between SCWT and performance: SiC devices optimized for low specific on-resistance ($R_{on,sp}$) suffer from short SCWT. In Ref. [7], SiC MOSFETs with increasingly short gate length show not only the desired reduction in $R_{on,sp}$ (~2.8x, from 21.5 mΩ·cm^2 to 7.5 mΩ·cm^2), but also a remarkable, undesired reduction in SCWT (~3.3x, from 9 µs to 2.7 µs). Data in [8] shows a similar trend. When the density of MOS-cells is increased, the $R_{on,sp}$ is improved, but the SCWT is strongly reduced. As mentioned earlier, smaller $R_{on,sp}$ leads to higher power-density and smaller conversion losses, but comes with a cost of smaller SCWT, due to faster thermal failure during short-circuit events.

Although several researchers have studied the short-circuit behavior of R&D SiC devices [9], the SCWT is not commonly reported and guaranteed in the datasheets of commercial SiC devices yet. To date, to the best of our knowledge, only one commercial SiC device datasheet reports SCWT, and it is limited to 3 µs [10], with no data available on specific R_{on}.

B. *Overview of GaN Devices*

An early research work by Nagahisa *et al.* [5] shows a 600-V GaN technology with a SCWT ≥ 3 µs at 400 V. However, according to the data reported in the paper, the normalized R_{on} of that technology is greater than 20 Ω·mm (> 9 mΩ·cm^2), relatively high to be adopted by the market.

So far, commercial 600-V GaN devices with competitive $R_{on,sp}$ have shown a SCWT ≥ 3 µs only if tested at relatively low voltages, in the range of 100-150 V [11]. When tested at 400 V, the SCWT of conventional 600-V GaN devices available in the market has been limited to less than 0.5 µs [11] [12].

Although the failure mechanisms are still object of research, the limited SCWT of commercial GaN HEMTs with competitive $R_{on,sp}$ could be ascribed to relatively high current densities. The source-drain channel forming at the AlGaN/GaN interface is a 2-dimensional electron gas (2DEG) with high charge-density (in the range of 10^{13} cm^{-2} electrons) and high mobility (as high as 2000 cm^2/V·s). The 2DEG gives GaN devices superior switching performance with respect to silicon and SiC devices, but it can also result in high current density (as high as 1 A/mm, depending on technology and material design), which, in turn, causes high power-density and a steep temperature rise during short-circuit events.

If the industry relies on conventional GaN HEMTs, non-ideal constrains would be needed for ultra-fast short-circuit protection circuitry [12] [13]. This scenario comes with very limited room for blanking-time and higher risks of false trigger in noisy industrial and automotive environments.

Alternatively, and preferably, engineering solutions can be implemented at a device-level to increase SCWT, while preserving high performance (low specific on-resistance and low switching time) and high reliability.

In this work, we report on an innovative solution for GaN power devices to achieve a SCWT equal to or greater than 3 µs at 400 V, while retaining competitive $R_{on,sp}$. This will allow the industry to use conventional short-circuit protection schemes, with sufficient immunity to noise and switching transients. The following sections discuss the device technology and the experimental results, including static and dynamic R_{on}, 400-V short-circuit, inductive switching, off-state leakage, and 1000-hour high-temperature reverse-bias stress.

III. SHORT-CIRCUIT CURRENT LIMITER (SCCL)

The solution presented in this work is based on the Transphorm normally-off two-chip core technology [14]. A low-voltage normally-off silicon FET is connected in cascode configuration with a high-voltage normally-on GaN HEMT. The Si-FET offers high threshold (+4 V) and highest gate reliability thanks to the robust SiO_2/Si MOS technology. The GaN HEMT is fabricated on silicon substrates for cost-effective manufacturing, and employs a field-plate structure to improve electric-field management and overall reliability. The field-plate is isolated with a dielectric layer to suppress leakage current and off-state losses. Transphorm core technology has been qualified with both JEDEC [15] and AEC-Q101 standards [16].

As mentioned in the Introduction, to achieve longer SCWT, the power dissipated during short-circuit events must be reduced, inhibiting the temperature rise and preventing the catastrophic failure. Lower power dissipated during short-circuit events can be achieved by reducing the short-circuit current flowing from drain to source. This solution has been patented for GaN devices [17] [18], and referred here to as Short-Circuit Current Limiter (SCCL) (Fig. 3). In a two-chip normally-off

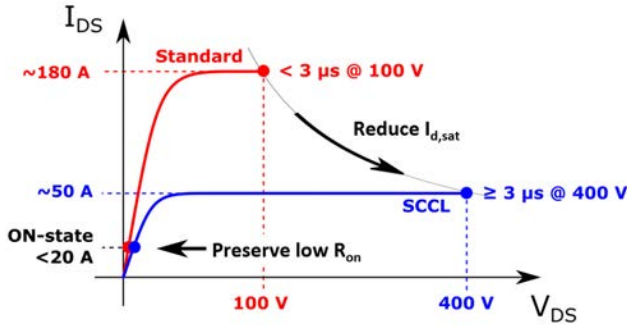

Fig. 3. The patented Short-Circuit Current Limiter (SCCL) acts to reduce the drain-source saturation-current ($I_{d,sat}$) to increase the SCWT of the device while preserving low on-state resistance.

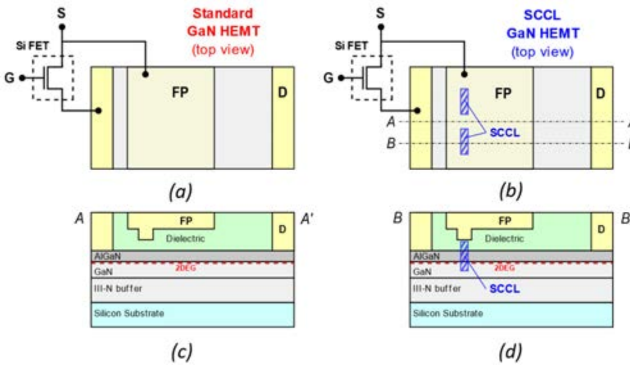

Fig. 4. Top-view of two-chip normally-off GaN switch *(a)* without and *(b)* with the patented Short-Circuit Current Limiter (SCCL). The SCCL is implemented by removing segments of the 2DEG channel along the width of the GaN HEMT. Longitudinal cross-sections taken along paths featuring *(c)* the current aperture, and *(d)* the current block. Drawings are not to scale.

solution, lower short-circuit current and higher SCWT can be achieved by controlling either the saturation-current ($I_{d,sat}$) of the Si-FET or the saturation-current of the GaN-HEMT. In this work, we report on the latter: increasing SCWT by reducing the $I_{d,sat}$ of the GaN-HEMT.

The SCCL was implemented on Transphorm's core technology by removing segments of the 2DEG channel along the width of the GaN-HEMT by using a proprietary process. The top-view of a standard GaN-HEMT and a GaN-HEMT with SCCL are shown in Fig. 4a and Fig. 4b, respectively. Longitudinal cross-sections of the SCCL device are shown in Fig. 4c and Fig. 4d. The section *AA'* is taken along current aperture path, where the 2DEG is uninterrupted from source to drain and electrons can flow in the on-state. In the aperture, the 2DEG properties (charge density & mobility) and the pinch-off voltage of the field-plate structure are the same as the standard device. The section *BB'* is taken along current-blocking path, showing the lack of 2DEG under a limited portion of the field-plate structure. The proper design of the current-blocking segmentation (length, width and periodicity of the current block areas) ensures a good control of the saturation current while maintaining a competitively low on-resistance.

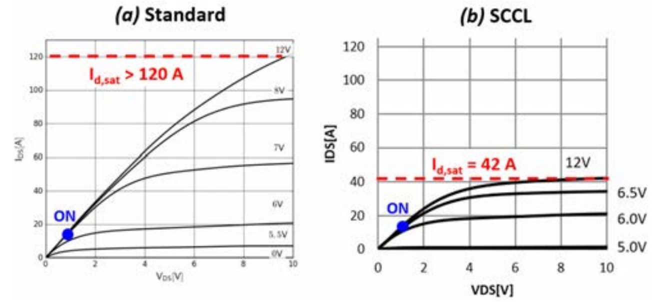

Fig. 5. Room-temperature output curves of *(a)* standard 650-V GaN device and *(b)* 650-V GaN device with SCCL. When the gate is fully on (V_{gs} = +12 V), the standard device has a saturation current ($I_{d,sat}$) that exceeds 120 A, whereas the device with the SCCL has a significantly lower $I_{d,sat}$ of 42 A. A 3x reduction in $I_{d,sat}$ is achieved. with only a 0.35x increase in on-resistance.

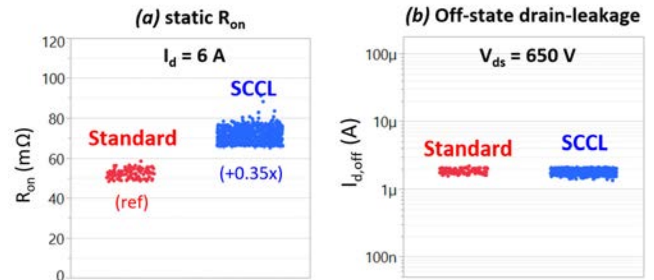

Fig. 6. *(a)* Virgin static R_{on} acquired at room temperature with an on-state I_d = 6 A. The SCCL device has a relatively small R_{on} penalty of +0.35x, as the current block is deployed only in a short section of the entire drain-source length. *(b)* Off-state drain leakage current acquired at V_{ds} = 650 V at room temperature. No increase in off-state leakage indicates that the SCCL technology does not degrade the quality of the field-plate dielectric isolation.

IV. Experimental Results

To demonstrate the benefits of the SCCL, we compare a standard GaN device [19] with a GaN device with SCCL. Both devices have the same chip-area, have the same 650-V rating, and have been packaged in 8x8 mm PQFN. Fig. 5 shows the room-temperature output characteristics: when the gate is fully on (V_{gs} = +12 V), the standard device has an average static R_{on} of 53 mΩ and a saturation current ($I_{d,sat}$) that exceeds 120 A, whereas the device with the SCCL has an average static R_{on} of 71 mΩ and a significantly lower $I_{d,sat}$ of 42 A. With the SCCL technology, we are able to achieve a 3x reduction in $I_{d,sat}$ with only a 0.35x increase in static on-resistance (Fig. 6a). This is possible because the R_{on} is mostly determined by the GaN-HEMT drain-access region (the equivalent of the "drift region" in a conventional power device), which is not affected by the SCCL blocking area. In fact, to control $I_{d,sat}$, it is sufficient to deploy the current block only in a small length along the entire source-drain spacing. It's worth noticing that, although the SCCL device has significantly lower $I_{d,sat}$ than the standard device, the SCCL $I_{d,sat}$ is still more than 2x higher than the maximum rated DC-current (20 A at room temperature). This is important to ensure not only good on-state operations, but also fast switching and fast discharge of the output capacitance (C_{oss}) during turn-on transients. Finally, the SCCL technology does not degrade the quality of the field-plate dielectric isolation, as

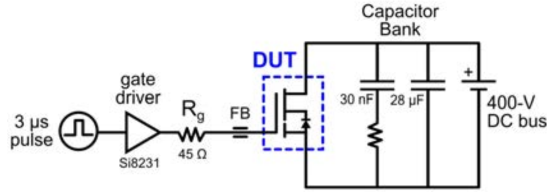

Fig. 7. Schematic of the short-circuit test-board. The board emulates an hard-switching fault, where the DUT is turned on directly onto a fault and experience the entire DC-bus voltage (400V) across its terminals.

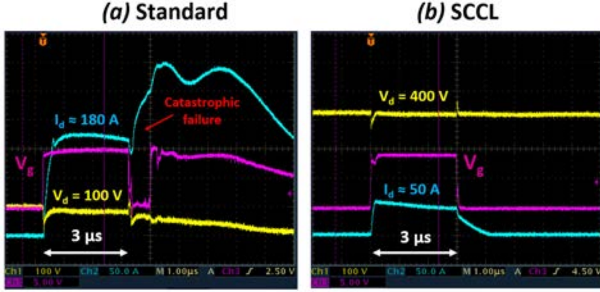

Fig. 8. 3-µs short-circuit pulses acquired at room-temperature on *(a)* a standard GaN device and *(b)* a GaN device with SCCL. The standard device shows a short-circuit current of 180 A and fails at a DC-bus voltage of 100 V, whereas the SCCL has a much lower short-circuit current (50 A) and survives a 3-µs pulse at 400 V.

no increase in 650-V off-state leakage current has been observed with respect to the standard device (Fig. 6b).

A. Short-Circuit Tests

To evaluate the SCWT improvement, we tested and compared devices with and without SCCL during short-circuit events. The short-circuit test-board is depicted in Fig. 7. The board applies a DC-bus directly to the drain of the DUT. A bank of capacitors is added on the drain-side to stabilize the DC-bus during switching. Short-circuit events are emulated by fully turning on the gate for 3 µs. To prevent damage to the instrumentation in case of catastrophic failure, we use an isolated gate-driver (Si8231). The gate resistor (R_g) is set to 45 Ω; if other R_g values are used, we do not expect major differences, as rise and fall time are only a negligible portion of the entire short-circuit pulse. During the test, the DC-bus is increased step-by-step from 50 V to 400 V with 50-V increments. At each step, we apply one short-circuit pulse and record the associated short-circuit waveforms (I_d, sensed with a current probe, V_d and V_g, sensed with voltage probes). This circuit is designed to evaluate the case referred to as “hard-switch fault,” where the DUT is turned on directly onto a fault. This is a worst-case scenario, as there is no voltage partitioning between multiple power devices: the DUT must withstand the entire 400-V bus voltage for the entire duration of the short-circuit pulse. The tests reported in this work have been carried out at room-temperature.

Results are shown in Fig. 8. The standard device shows a short-circuit current of 180 A and fails after 3 µs at a DC-bus voltage of only 100 V, whereas the SCCL device has a much lower short-circuit current (50 A) and survives a 3-µs pulse at a voltage of 400 V. This remarkable increase in short-circuit robustness (of more than 4x) demonstrates the proof-of-concept and the successful implementation of the SCCL design, goal of this work.

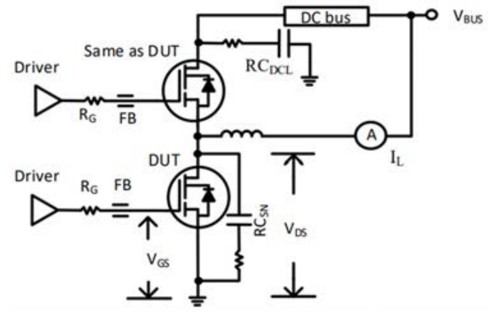

Fig. 9. Schematics for the inductive switching test-board.

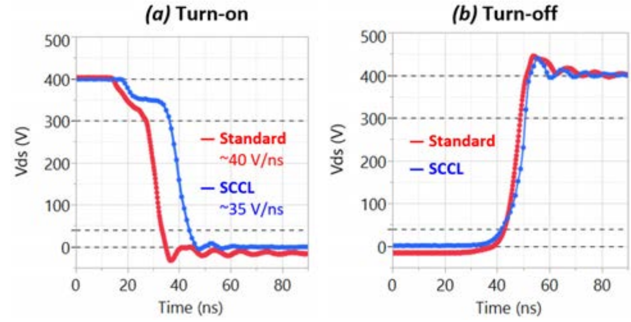

Fig. 10. *(a)* Turn-on and *(b)* turn-off transients acquired with an inductive load current of ~15 A for both the standard device and the SCCL device. The SCCL device has similar *dv/dt* than the standard device, indicating that the low $I_{d,sat}$ of the SCCL does not hamper the charging and discharging of the output capacitance (C_{oss}).

B. Dynamic R_{on} and switching time

In order to assess the dynamic performance of the SCCL device, we carried out dynamic R_{on} tests and inductive switching tests. The dynamic R_{on} tests were carried out with a resistive load of 80 Ω at a DC-bus of 480 V. On-state pulse-width and duty-cycle are 2 µs and 0.01% respectively. The device remains in the off-state for most of the test time. The dynamic R_{on} value is recorded after 60 s of operation to ensure the filling of the traps (if any). Results show that the relative increase between dynamic and static R_{on} is approximately +18%. This is similar to the relative increase between dynamic and static R_{on} in standard devices and indicates that the SCCL blocking region does not exacerbate charge-trapping.

The inductive switching test was carried out with a DC-bus of 400 V and an inductive load of 40 µH. The circuit uses two identical DUTs: one on the low-side, switched between off-state and on-state, and one on the high-side, used in reverse-conduction mode to recycle the inductor current. In the gate loop of both devices, there is an R_g of 50 Ω and a ferrite beads of 240 Ω at 100MHz. Snubbers with values of (33 pF + 15 Ω) and (10 nF + 10 Ω) x 2 are applied to the switching node and DC-bus,

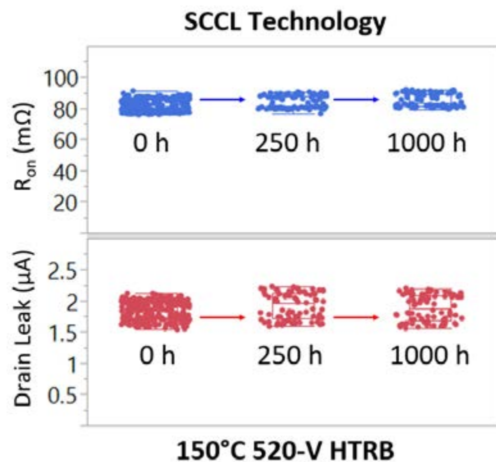

Fig. 11. R_{on} and drain leakage measured before and after 1000-h HTRB test carried out at 150°C and 520 V on SCCL GaN devices (80 parts). After both 250 and 1000 hours, we observed no fuse failure, no leakage increase, and a relatively small parametric R_{on} degradation (~5%). The small parametric R_{on} degradation is similar to what observed in standard devices, therefore indicating that the SCCL blocking region does not introduce any additional degradation and/or failure mechanisms.

respectively (Fig. 9). The inductor current is ramped from 0 A to 15 A with multiple on-state pulses applied to the low-side DUT. The test has been carried out with a pair of standard devices and a pair of SCCL devices. Fig. 10a and Fig. 10b shows the switching node waveforms during turn-on and turn-off transients at a load current of ~15 A. During both turn-on and turn-off, the pair of SCCL devices have similar *dv/dt* than the standard devices (≥35 V/ns with R_g = 50 Ω), indicating that the low $I_{d,sat}$ of the SCCL does not hamper the charging and discharging of the output capacitance (C_{oss}).

C. Reliability

In order to assess the reliability of the SCCL device, we submitted 80 parts to a High-Temperature Reverse-Bias (HTRB) at 150°C and 520 V for 1000 hours. Full parametric characterization has been carried out at the beginning (t = 0 h), interim (t = 250 h), and at the end of the stress campaign (t = 1000 h). Results are reported in Fig. 11. After both 250 hours and 1000 hours, we observed no fuse failure, no leakage increase, and a relatively small parametric R_{on} degradation (~5%). The small parametric R_{on} degradation is similar to what observed in standard devices, therefore indicating that the SCCL blocking region does not introduce any additional degradation and/or failure mechanisms. This is a promising result towards the prospective JEDEC and automotive qualifications of SCCL technology.

V. Conclusions

In this work, we have presented a high-performance high-reliability solution to improve the short-circuit withstanding time of GaN-based power devices to 3 µs at 400 V with a limited increase in on-resistance. The Short-Circuit Current Limiter (SCCL) reduces the short-circuit current by more than 3x and improves short-circuit robustness by more than 4x. As of today, the penalty in on-resistance is limited to 0.35x. Further reduction of the R_{on} penalty can be achieved by continuous optimization of the SCCL design. From an initial characterization campaign including dynamic R_{on} tests, inductive switching tests, and 100-h HTRB, the SCCL technology has demonstrated to have the similar switching performance and reliability than the standard Transphorm technology.

The SCCL technology can be applied to the entire portfolio of GaN products to serve a broad range of motor drive applications. Thanks to extended SCWT, the SCCL technology will allow the industry to adopt conventional short-circuit protection schemes, with sufficient immunity to noise and switching transients.

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